WHAT IS CLAIMED IS:

1. A nonvolatile semiconductor memory device comprising:

a floating gate formed on a semiconductor substrate via a gate insulating film;

diffused layers, as sources or drain regions, which are positioned on opposite sides of the floating gate and which are formed in the semiconductor substrate;

first and second control gates which are formed on the opposite sides of the floating gate and which drive the floating gate; and

an inter-gate insulating film which insulates the first and second control gates from the floating gate and diffused layers.

2. The device according to claim 1, wherein the inter-gate insulating film contacts opposite side walls of the floating gate and lower surfaces of the first and second control gates, and the first and second control gates are disposed opposite to the diffused layers.

3. The device according to claim 1, wherein the inter-gate insulating film includes first and second portions, the first portion contacts the floating gate, the second portion contacts the lower surface of the first or second control gate, and a thickness of the second portion is larger than that of the first

portion.

4. The device according to claim 3, wherein the first portion is a stacked film including a silicon nitride film, and the second portion is a silicon oxide film.

5. The device according to claim 3, wherein the first portion is a single layer or stacked film containing aluminum oxide, and the second portion is a silicon oxide film.

6. The device according to claim 3, further comprising:

insulating materials which are formed on opposite side-surface sides disposed opposite to the diffused layers of the floating gate and which insulate adjacent memory cells;

first and second trenches formed in the insulating materials on the diffused layers; and

conductive materials which are formed in the first and second trenches to constitute the first and second control gates,

wherein the first and second control gates of the adjacent memory cells are connected via the conductive materials.

7. The device according to claim 4, further comprising:

a third trench which is formed opposite to a side surface different from that in contact with the first

and second control gates of the floating gate; and

a second insulating material embedded in the third trench,

wherein bottom surfaces of the first and second control gates on the second insulating material in the third trench are higher than those of the first and second control gates on the semiconductor substrate.

8. A nonvolatile semiconductor memory device comprising:

a trench formed in a semiconductor substrate;

a floating gate formed in a bottom portion of the trench via a first gate insulating film;

diffused layers, as sources or drain regions, which are formed in the semiconductor substrate on opposite sides of the floating gate; and

first and second control gates which are positioned on the opposite diffused layers and which are formed on opposite side walls of the floating gate via an inter-gate insulating film and which drive the floating gate.

9. The device according to claim 8, further comprising:

a second gate insulating film formed between the first and second control gates and the semiconductor substrate,

wherein the inter-gate insulating film contacts the opposite side walls of the floating gate, and the

second gate insulating film is thicker than the inter-gate insulating film.

10. The device according to claim 8, wherein the first gate insulating film contacts the bottom portion and side surfaces of the floating gate.

11. The device according to claim 8, wherein the inter-gate insulating film contacts the opposite side walls of the floating gate, the third gate insulating film is disposed between the side surfaces of the trench and the floating gate, and the first gate insulating film, inter-gate insulating film, and third gate insulating film formed in the bottom surface of the floating gate have different film thicknesses.

12. The device according to claim 11, wherein assuming that the film thickness of the inter-gate insulating film is T1, that of the third gate insulating film is T2, and that of the first gate insulating film is T3, a relation among these is $T1 > T2 > T3$.

13. The device according to claim 12, further comprising:

a trench formed opposite to a side surface different from that disposed opposite to the first and second control gates of the floating gate; and

a first insulating material embedded in the trench,

wherein the upper surfaces of the first and second

control gates are formed to be lower than the upper surface of the first insulating material.

14. The device according to claim 13, further comprising:

second insulating materials formed in upper parts of the first and second control gates;

first and second openings which are formed opposite to the first and second control gates in the second insulating materials and whose areas are smaller than those of the upper surfaces of the first and second control gates; and

first and second wirings connected to the first and second control gates via the first and second openings.

15. The device according to claim 14, wherein the first and second control gates are set to different potentials.

16. The device according to claim 14, wherein the film thickness of the inter-gate insulating film is larger than that of the gate insulating film.

17. The device according to claim 14, wherein the inter-gate insulating film is formed by a stacked film containing any one or at least two of aluminum oxide, hafnium oxide, silicon oxide, silicon nitride, and zirconia oxide.

18. The device according to claim 14, wherein the second insulating material is formed by a single layer

of silicon nitride or a stacked film containing silicon nitride.

19. The device according to claim 14, wherein the floating gate and first and second control gates are formed of polysilicon.

20. The device according to claim 14, wherein the first and second control gates are formed by a stacked film containing any one or at least two of titanium, tungsten, tungsten nitride, and titanium nitride.

21. The device according to claim 14, wherein the control gate includes a salicide structure of titanium, cobalt, or nickel metal.

22. The device according to claim 14, wherein the bottom surface of the floating gate is positioned below that of the control gate.

23. The device according to claim 14, wherein when the first and second control gates have the same potential, a capacitance ratio (Cr) to determine a potential of the floating gate is represented by the following equation:

$$Cr = Cip/(Cip+Ctox)$$
$$= (2\bullet\varepsilon ip\bullet W\bullet Tfg/Tip)/((2\bullet\varepsilon ip\bullet W\bullet Tfg/Tip) + \varepsilon tox\bullet W\bullet L/Ttox),$$

wherein εip: a permittivity of the inter-gate insulating film, εtox: permittivity of the gate insulating film, W: channel width of the cell transistor, L: gate length of the cell transistor,

Tfg: FG film thickness, Ttox: film thickness of the gate insulating film, and Tip: film thickness of the inter-gate insulating film.

24. A nonvolatile semiconductor memory device comprising:

a floating gate formed above a semiconductor substrate;

first and second control gates which are formed on opposite sides of the floating gate and which are insulated from the floating gate and semiconductor substrate;

a first capacitance between the semiconductor substrate and floating gate;

a second capacitance between the first control gate and floating gate;

a third capacitance between the second control gate and floating gate;

a fourth capacitance between the first control gate and semiconductor substrate; and

a fifth capacitance between the second control gate and semiconductor substrate.

25. A nonvolatile semiconductor memory device comprising:

a cell transistor comprising a floating gate, source, and drain; and

first and second control gates which are disposed on opposite sides of the floating gate of the cell

transistor,

wherein the floating gate is selected by the first and second control gates.

26. A nonvolatile semiconductor memory device comprising:

cell transistors which comprise a floating gate, source, and drain and in which the adjacent sources and drains are connected in series;

control gates disposed on opposite sides of the floating gate of each of the cell transistors;

a first selection gate connected between one end of the cell transistors and bit line; and

a second selection gate connected between the other end of the cell transistors and source line,

wherein the control gates on the opposite sides of the floating gate select the floating gate.

27. The device according to claim 26, wherein the floating gate is selected by two adjacent control gates.

28. A memory card including the nonvolatile semiconductor memory device recited in claim 1.

29. A cardholder to which the memory card recited in claim 28 is inserted.

30. A connecting device to which the memory card recited in claim 29 is inserted.

31. The connecting device according to the claim 30, wherein the connecting device is configured

to be connected to a computer.

32. A memory card including the nonvolatile semiconductor memory device recited in claim 1 and a controller which controls the nonvolatile semiconductor memory device.

33. A cardholder to which the memory card recited in claim 32 is inserted.

34. A connecting device to which the memory card recited in claim 32 is inserted.

35. The connecting device according to the claim 34, wherein the connecting device is configured to be connected to a computer.

36. An IC card including the nonvolatile semiconductor memory device recited in claim 1.

37. The IC card including a controller which controls the nonvolatile semiconductor memory device recited in claim 1.

38. A USB memory system according to claim 1, comprising:

a USB memory device having the nonvolatile semiconductor memory device recited in claim 1,

a first controller which controls the nonvolatile semiconductor memory device; and

a first connector connected to the first controller.

39. The USB memory system according to claim 38, further comprising:

a host platform including a second connector which is connected to the first connector of the USB memory device, and a controller connected to the second connector, which controls the USB memory system.